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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/085,919	02/28/2002	Albrecht Mayer	J&R-0819	1176
24131	7590 02/09/2005		EXAMINER	
LERNER AND GREENBERG, PA P O BOX 2480			BRITT, CYNTHIA H	
	HOLLYWOOD, FL 33022-2480		ART UNIT	PAPER NUMBER
		•	2133	
			DATE MAILED: 02/09/2005	

Please find below and/or attached an Office communication concerning this application or proceeding.

		Application No.	Applicant(s)			
		10/085,919	MAYER ET AL.			
	Office Action Summary	Examiner	Art Unit			
		Cynthia Britt	2133			
Period f	The MAILING DATE of this communication ap or Reply	pears on the cover sheet with the c	orrespondence address			
THE - Exte after - If th - If NO - Failt Any	MORTENED STATUTORY PERIOD FOR REPL MAILING DATE OF THIS COMMUNICATION. ensions of time may be available under the provisions of 37 CFR 1. If SIX (6) MONTHS from the mailing date of this communication. If period for reply specified above is less than thirty (30) days, a reploperiod for reply is specified above, the maximum statutory period ure to reply within the set or extended period for reply will, by statut reply received by the Office later than three months after the mailing patent term adjustment. See 37 CFR 1.704(b).	136(a). In no event, however, may a reply be timely within the statutory minimum of thirty (30) days will apply and will expire SIX (6) MONTHS from the cause the application to become ABANDONE	nely filed s will be considered timely. the mailing date of this communication. D (35 U.S.C. § 133).			
Status						
1)⊠	Responsive to communication(s) filed on 22 f	November 2004.				
2a)⊠	This action is <b>FINAL</b> . 2b) ☐ Thi	s action is non-final.				
3)□	Since this application is in condition for allowance except for formal matters, prosecution as to the ments is closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.					
Disposit	tion of Claims					
5)□	<ul> <li>✓ Claim(s) 1-8,10 and 11 is/are pending in the application.</li> <li>4a) Of the above claim(s) is/are withdrawn from consideration.</li> <li>☐ Claim(s) is/are allowed.</li> <li>✓ Claim(s) 1-4,8,10 and 11 is/are rejected.</li> <li>✓ Claim(s) 5-7 is/are objected to.</li> </ul>					
Applicat	tion Papers					
10)⊠	The specification is objected to by the Examine The drawing(s) filed on <u>28 February 2002</u> is/an Applicant may not request that any objection to the Replacement drawing sheet(s) including the correct The oath or declaration is objected to by the Examine The specification is objected.	re: a) ☐ accepted or b) ☒ objecte e drawing(s) be held in abeyance. See ction is required if the drawing(s) is obj	e 37 CFR 1.85(a). jected to. See 37 CFR 1.121(d).			
Priority	under 35 U.S.C. § 119					
12)⊠ a)	Acknowledgment is made of a claim for foreign All b) Some * c) None of:  1. Certified copies of the priority document copies of the priority document copies of the priority document copies of the certified copies of the priority document copies of the certified copies of the priority copies of the	nts have been received. Its have been received in Applicationity documents have been received in Application (PCT Rule 17.2(a)).	on No ed in this National Stage			
Attachmer	• •	o.∇				
	ce of References Cited (PTO-892) ce of Draftsperson's Patent Drawing Review (PTO-948)	4) ⊠ Interview Summary Paper No(s)/Mail Da				
3) 🔲 Infor	rmation Disclosure Statement(s) (PTO-1449 or PTO/SB/08 or No(s)/Mail Date		Patent Application (PTO-152)			

#### **DETAILED ACTION**

Claims 1-8, 10 and 11 are presented for examination.

The examiner would like to thank applicant for willingness to expedite prosecution of this case. However, since the interview, new art has been discovered and applied. Therefore, the examiner will leave the corrections for applicant in a subsequent response, and the discussed items will not be objected to/ rejected in this office action.

## **Drawings**

The drawings were objected to in a prior office action as below:

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the method of claims 8-11 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

The examiner would like to point out that method claims are typically illustrated by a simple flowchart(s) with the boxes containing the steps of the method. These drawings aid in the understanding of the claimed invention.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

### Response to Arguments

Applicant's arguments with respect to claims 1-8 and 10-11 have been considered but are most in view of the new ground(s) of rejection.

## Allowable Subject Matter

Claims 5-7 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

### Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4, 8 and 10-11 are rejected under 35 U.S.C. 102(b) as being anticipated by Spix et al. U.S. Patent No. 5,253,359.

As per claim 1, Spix et al. teach a control and maintenance architecture providing an integrated hardware and software solution to the problem of access to and control over the internal machine registers of a highly parallel multiprocessor system. (Column 3 lines 34-38) The use of scan path elements and functions are implemented (Column 8 lines 17-20). If an error (predetermined event) is detected in the clusters, machine state information is saved by the scan paths, and is gathered by the MCUs. It is important

Application/Control Number: 10/085,919

Art Unit: 2133

that the information is read from the scan paths by the MCUs as quickly as possible, since a subsequent error in the cluster may overwrite the previous error before it can be gathered. For example, if a single bit memory error is detected, the scan paths can latch the entire machine state for subsequent analysis (Column 8 lines39-48)

As per claims 2 and 3, Spix et al. teach controlling the operation of the system such as starting, stopping, or n-stepping the master clock, setting or sensing internal machine states, executing diagnostic routines, and capturing errors at run-time for later display and analysis (Column 2 lines 26-36).

As per claim 4, Spix et al. teach that an operator can control the operation of the system such as starting, stopping, or n-stepping the master clock, setting or sensing internal machine states, executing diagnostic routines, and capturing errors at run-time for later display and analysis (Column 2 lines 26-36).

As per claims 8 and 10, Spix et al. teach a control and maintenance architecture providing an integrated hardware and software solution to the problem of access to and control over the internal machine registers of a highly parallel multiprocessor system.

(Column 3 lines 34-38) The use of scan path elements and functions are implemented (Column 8 lines 17-20). If an error (predetermined event) is detected in the clusters, machine state information is saved by the scan paths, and is gathered by the MCUs. It is important that the information is read from the scan paths by the MCUs as quickly as possible, since a subsequent error in the cluster may overwrite the previous error before it can be gathered. For example, if a single bit memory error is detected, the scan paths can latch the entire machine state for subsequent analysis (Column 8 lines39-48)

Art Unit: 2133

As per claim 11, Spix et al. also teach that an operator can control the operation of the system such as starting, stopping, or n-stepping the master clock, setting or sensing internal machine states, executing diagnostic routines, and capturing errors at run-time for later display and analysis (Column 2 lines 26-36).

#### Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

JP 63081552 A Masumura Takashi

This patent teaches that to reduce the analysis time of error analysis and to attain accurate analysis a method of holding the interface state if an error takes place in an interface dialog with peripheral equipment and collecting error information. A channel device is provided with an interface control section and if an error takes place, the interface state is held, interrupt is given to the control firmware, the state of the internal flip-flop is collected by a scan path, the holding is released after the end of collection to restart the stopped dialog. Thus, the state of the hardware of the interface dialog at the point of time of occurrence of error is grasped accurately, the analysis time is decreased, and accurate analysis is attained.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

Page 6

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cynthia Britt whose telephone number is 571-272-3815. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Application/Control Number: 10/085,919

Art Unit: 2133

Page 7

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Cynthia Britt
Examiner
Art Unit 2133

SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100